REMARKS

Before entry of this amendment, claims 1-21 were pending. In the Office Action, claims 1-3, 8 and 20 were rejected, and claims 4 and 7 were objected to. Claims 5-6, 9-19 and 21 are allowed. In the present amendment, claim 22 is added, and no claims are amended. After entry of the amendment, claims 1-22 are pending.

Reconsideration and allowance is respectfully requested.

I. Rejection of claims 1-3, 8 and 20

Claims 1-3, 8 and 20 are rejected under 35 U.S.C. §102(e) as being anticipated by Hirai (US Pub No. 2002/0180540) (Office Action, p. 2, lines 16-17).

A. Independent claim 1

The Examiner states, with regard to claim 1, that "Hirai discloses, in Figure 1, a circuit and its corresponding method comprising the steps of a) determining [11] a cycle period of first clock signal [reference signal]; b) detecting [11] rising and falling edges of a second clock signal [feedback signal] during the cycle period the first clock signal; and c) designating the cycle period of the first clock signal as valid when a single rising edge *(Fig. 2, tNA+1)* of the second clock signal and a single falling edge *(Fig. 2, a)* of the second clock signal are detected during the cycle period of the first clock signal." (Office Action, p. 2, lines 18-24, italics in original). Applicants respectfully disagree.

Hirai does not form the basis for a valid rejection under § 102(e) because Hirai does not disclose all of the elements of claim 1. Hirai does not disclose the third element recited in claim 1:

> "designating the cycle period of the first clock signal as valid when a single rising edge of the second clock signal and a single falling

> edge of the second clock signal are detected during the clock period of the first clock signal."

The Examiner argues that Hirai discloses the step of designating a cycle period as valid when a single rising edge and a single falling edge of a second clock signal are detected during a clock period of a first clock signal. (Office Action, p. 2, lines 21-24) As support, the Examiner points to the circuit diagram of figure 1 and to the waveform diagram of figure 2 that shows a rising edge "tNA+1" and a falling edge "a" of a feedback signal. Neither the circuit diagram of figure 1, nor the waveform diagram of figure 2, of Hirai discloses any steps or any method.

Although the rising edge "tNA+1" and the falling edge "a" of the feedback signal happen to be shown in figure 2 as occurring during cycle "NA" of the reference signal, the circuit of figure 1 of Hirai does not detect whether a single rising edge "tNA+1" and a single falling edge "a" of the feedback signal occur during cycle "NA" of the reference signal. In addition, Hirai does not designate whether cycle "NA" of the reference signal is valid. Indeed, Hirai counts the falling edge "a" of the feedback signal only if a predetermined value "NA" of cycles of both the feedback signal and the reference signal is reached. At other times, falling edge "a" is not detected, and cycles of the reference signal cannot be designated as either valid or invalid. The counter 24 of Hirai that counts falling edge "a" is reset when "NA" cycles of both the feedback signal and the reference signal have not been counted. (See Hirai at ¶ [0055]).

Whether "NA" cycles of both the feedback signal and the reference signal is reached is determined in Hirai by counting rising edges. Hirai states, "The first counter 21 counts up on the rising edge of the inputted feedback signal. The second counter 22 counts up on the rising edge of the inputted reference signal" (Hirai at ¶ [0034]). Then, if cycle "NA" of both the feedback signal and the reference signal is reached, the falling edge "a" of the feedback signal is counted regardless of whether falling edge "a" plus a single rising edge of the feedback signal both fall within cycle "NA" of the reference signal. The lock detection

circuit of Hirai does not detect when a single rising edge and a single falling edge of the feedback signal occur during a particular cycle of the reference signal. Thus, Hirai does not detect when a particular cycle of either the feedback signal or reference signal is valid.

Hirai cannot detect an unlocked state in cycles before cycle "NA" of the feedback signal. Hirai states, "An unlock state can be detected in each NA cycle of the feedback signal" (Hirai at ¶ [0063]). Even for the particular cycle "NA" of the feedback signal, the circuit of figure 1 of Hirai does not indicate whether the single rising edge and the single falling edge of feedback signal cycle "NA" both occur during the reference signal cycle "NA". Therefore, the circuit of figure 1 of Hirai does not indicate whether the particular reference signal cycle "NA" is valid.

Although the third counter (24) of Hirai counts the falling edge "a" of the feedback signal after "NA" rising edges of both the feedback signal and the reference signal are counted, the third counter (24) counts the falling edge "a" even when reference signal cycle "NA" is not valid. For example, the third counter (24) counts the falling edge "a" of the feedback signal even when the rising edge "tNA" of the feedback signal occurs before reference signal cycle "NA" and rising edge "tNA+1" of the feedback signal occurs after reference signal cycle "NA" (a single falling edge but no rising edge). Moreover, the third counter (24) counts the falling edge "a" of the feedback signal even when the rising edge "tNA" of the feedback signal occurs during reference signal cycle "NA" and rising edge "tNA+1" of the feedback signal also occurs during reference signal cycle "NA" (a single falling edge and two rising edges). Thus, the counting of rising and falling edges of the feedback signal in Hirai does not indicate whether a cycle of the reference clock is valid, and Hirai discloses no steps or method for designating a cycle period as valid.

Because Hirai does not disclose all of the elements of claim 1, reconsideration of the § 102(e) rejection and allowance of claim 1 is requested.

B. Dependent claims 2-3 and 8

Claims 2-3 and 8 depend from claim 1.

Dependent claim 2 is rejected as being anticipated by Hirai. (Office Action, p. 3, lines 1-2.) Claim 2 depends from claim 1, and Applicants respectfully submit that claim 2 is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 2 is requested.

Dependent claim 3 is rejected as being anticipated by Hirai. The Examiner states, with regard to claim 3, that "Hirai discloses, in Figure 1, that the determining the cycle period of the first clock signal further comprises detecting [11] a rising edge of the first clock signal and detecting [11] an immediately following rising edge the first clock signal." (Office Action, p. 3, lines 3-5.) Applicants disagree. Although the circuit in Hirai counts rising edges of the reference signal, the circuit in Hirai does not determine the cycle period of the reference signal. Hirai does not disclose a method for determining whether a single rising edge and a single falling edge of the feedback signal occur after a rising edge and before the immediately following rising edge of the reference signal. The Examiner has not pointed to any step of Hirai that determines whether a single rising edge of the feedback signal occurs after a rising edge and before the immediately following rising edge of the reference signal.

The Examiner points to the waveform diagram of figure 2 of Hirai. But figure 2 does not disclose any steps. Figure 2 does not disclose a step of (i) determining whether rising edge "tNA+1" occurs after the rising edge and before the immediately following rising edge that define cycle "NA" of the reference signal and (ii) determining whether rising edge "tNA+1" is the only rising edge that occurs after the rising edge and before the immediately following rising edge that define cycle "NA".

The Examiner also points to the phase comparator (11) shown in the circuit diagram of figure 1 of Hirai. The phase comparator (11) does not disclose a step of determining whether a single rising edge and a single falling edge of the

feedback signal occur after a rising edge of the reference signal and before the immediately following rising edge of the reference signal. Moreover, the phase comparator (11) does not perform such a function. The Examiner has not pointed to any circuitry of Hirai that, after counting falling edge "a" of the feedback signal, determines whether rising edge "tNA+1" occurs after the rising edge and before the immediately following rising edge that define reference signal cycle "NA" in figure 2.

Because Hirai does not disclose all of the elements of claim 3, reconsideration of the § 102(e) rejection and allowance of claim 3 is requested. In addition, claim 3 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 3 is requested.

Dependent claim 8 is rejected as being anticipated by Hirai. (Office Action, p. 3, lines 6-9.) Claim 8 depends from claim 1, and Applicants respectfully submit that claim 8 is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claim 8 is requested.

C. Dependent claims 4 and 7

Claims 4 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. (See Office Action, p. 3, lines 20-22.) Claims 4 and 7 depend from claim 1, and Applicants respectfully submit that claims 4 and 7 are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration and allowance of claims 4 and 7 is requested.

D. Independent claim 20

Claim 20 is rejected under 35 U.S.C. § 102(e) as being anticipated by Hirai. (Office Action, p. 3, lines 10-17.) Claim 20 recites:

> ". . . wherein the means detects that the feedback clock signal and the reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period and when a single rising edge and a single falling edge of the feedback clock signal are detected during less than a predetermined number of the reference clock cycles during the time period."

The rejection of claim 20 under § 102(e) should be withdrawn because Hirai does not disclose all of the limitations of amended claim 20.

First, Hirai does not disclose a means that detects that a feedback clock signal and a reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period. To the contrary, the circuit in Hirai indicates a locked state when the count of the number of rising edges of the feedback clock and the count of the number of rising edges of the reference clock are both equal to a predetermined set value "NA" at a particular point in time.

Second, Hirai does not disclose a means for detecting when a single rising edge and a single falling edge of the feedback clock signal occur during less than a predetermined number of the reference clock cycles. The Examiner points to paragraph [0062], lines 14-16, of Hirai, which states, "The third counter 24 performs a count operation on the falling edge of the feedback signal." Third counter 24, however, counts the falling edge of the feedback signal regardless of whether the falling edge and a single rising edge of the feedback signal occur before the end of a predetermined number of reference clock cycles.

During cycles of the reference clock before cycle "NA" of figure 2, the falling edge of the feedback signal is not counted at all. Hirai states, "[W]hen the first counter 21 counts the feedback signal by "NA" . . . and the count value of the second counter 22 as the reference signal is not "NA", the third counter 24 is reset to restart a count operation of the feedback signals from the count value "0" of the third counter 24." (Hirai at ¶ [0063])

As shown in figure 2 of Hirai, falling edge "a" is counted only if (i) counter 21 counts "NA" rising edges of the feedback signal and (ii) counter 22 counts "NA" rising edges of the reference signal and then, in the event of (i) and (ii), falling edge "a" is counted regardless of whether rising edge "NA+1" of the feedback signal occurs within cycle "NA" of the reference signal or after cycle "NA" of the reference signal. Hirai states, "While . . . (the count values of the first an second counters 21 and 22 are NA), the output signal of the second AND circuit 27 is at High level. . . . The third counter 24 is allowed to be in a count enable state to count up upon falling transition of the feedback signal. With the timing a of FIG. 2 (the falling timing from High level to Low level of the feedback signal), the first and second counters 21 and 22 have not been reset yet." (Hirai, ¶ [0060], emphasis added) Thus, the third counter 24 counts up upon the falling transition of the feedback signal regardless of which of counters 21 or 22 is subsequently reset first, and consequently regardless of whether rising edge "NA+1" of the feedback signal occurs within or outside of cycle "NA" of the reference signal.

The circuit in Hirai does not detect that a feedback clock signal and a reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period. In addition, although the circuit in Hirai counts a falling transition of the feedback signal in certain situations, the circuit in Hirai does not detect when a single rising edge and a single falling edge of the feedback clock signal occur during less than a predetermined number of the reference clock cycles. Because Hirai does not disclose all of the elements of claim 20, reconsideration of the § 102(e) rejection and allowance of claim 20 is requested.

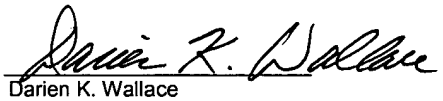
II. New claim 22

Applicants are adding new claim 22, which is supported by the specification and allowable over the cited references. No new matter is added.

III. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that the entire application (claims 1-22 are pending) is in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the Examiner is requested to contact the undersigned at (925) 621-2121.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By 
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